REMARKS

Attached hereto is an excess claims fee letter and fee for one excess independent claim.

Claims 1-19 are all of the claims presently pending in the application. New claims 15-19 are added. Claims 1-4, 6-9, and 11-14 stand rejected on prior art grounds.

Claims 5 and 10 stand rejected under 35 USC §112, second paragraph, as indefinite. Applicant believes that the above claim amendments correct the problem addressed by this indefiniteness rejection and respectively requests that the Examiner reconsider and remove this rejection.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Regarding the prior art rejections, claims 1-4, 8, 9, 13, and 14 stand rejected under 35 U.S.C. §102(b) as anticipated by US Patent 5,742,842 to Suetake. Claims 6, 7, 11, and 12 stand rejected as unpatentable over Suetake. Because claims 5 and 10 have no associated prior art rejection, it is presumed that these two claims would be allowable if the indefiniteness issue is resolved and if rewritten in independent format.

These prior art rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example, in independent claim 1, is directed to a computer system which includes a plurality of memory banks. A processor unit controls an overall processing of an operation. Additional processing units, each of which corresponds to one of the memory banks, performs a part of the operation independently of the processor unit. The operation is performed by the additional processing units, using data stored in the corresponding memory banks and based on an instruction or data provided from the processor unit.

As explained on page 2 of the specification, conventional methods of parallel processing, such as demonstrated by the cited prior art Suetake, share a common memory area for the multiple processors, thereby making it difficult to guarantee that data or counting will not be contaminated during parallel or vector processing.

In contrast, by uniquely associating each additional processing unit with its own independently-functioning memory bank, the additional processing unit can lock-out access to its associated memory bank during the period it is processing its part of the operation, thereby safeguarding the information content without additional computer programming techniques that are required when using a single memory area for all the processors (e.g., as used in Suetake). Moreover, as explained beginning at line 2 of page 25 and continuing through the final line on page 28, the associated memory banks of the present invention provides vectorization and/or parallelization capability beyond the conventional techniques described in these pages.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Suetake anticipates the present invention defined by claims 1-4, 8, 9, 13, and 14 and renders obvious claims 6, 7, 11, and 12. Presumably, since there are no prior art rejections for claims 5 and 10, these two claims are allowable over Suetake, once the indefiniteness issue has been resolved.

Applicant respectfully traverses that Suetake teaches or reasonably suggests the unique computer architecture defined by the independent claims. That is, the present invention incorporates a feature that each additional processing unit is associated with its own memory bank. This feature allows each additional processing unit to lock out its associated memory bank during the time it is processing data, thereby providing a simple method of guaranteeing data and counting integrity for vectorization and parallelization.

For example, as explained in the first full paragraph on page 25 of the specification, the present invention addresses the problem in which an array "count" or two-dimensional array "list" can be incorrectly updated.

Suetake fails to incorporate this design approach of localized, automonous memory units for each slave processor. That is, as clearly shown in Figure 8, the slave processor 802 and CPU 801 share access to the main cache 805 and main memory unit 806.

In the rejection currently of record, the Examiner relies upon the architecture shown in Figure 10 as corresponding to the description of the independent claims. However, the processing pipelines and/or internal registers shown in Figure 10, upon which the Examiner seems to consider as equivalent to the "memory banks" of the claimed invention, are internal to the slave processor 802 and are somewhat analogous to the internal registers 33-38 of the additional processors 30, as shown in Figure 3 of the present disclosure.

Applicant submits that, to one of ordinary skill in the art, these operating registers, internal to a processing unit, are not equivalent to the term "memory bank". That is, Applicant submits that one of ordinary skill in the art would consider this terminology as a term of art and that a "memory bank" is not at all equivalent to an internal operating register or an operational pipeline.

Although the Examiner is allowed to make a reasonably broad interpretation, that interpretation must be consistent with an interpretation that one of ordinary skill in the art would agree, as clearly stated in MPEP §2111: "*The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach.*"

For at least the reasons stated above, Applicant respectfully submits that Suetake fails to teach or suggest every feature of the independent claims and, indeed, clearly demonstrates exactly the problem being addressed by the present invention for parallel processing that uses a common memory area.

Hence, turning to the clear language of the claims, in Suetake there is no teaching or suggestion of: "...additional processing units, each of which corresponds to one of the memory banks ....", as required by claim 1. The remaining independent claims have similar language.

Therefore, the Examiner is respectfully requested to withdraw these rejections based on Suetake.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Suetake, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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